STAR Cryoelectronics

pcSQUID™ User's Manual

PCS800 Control Software

Programmable Feedback Loop
Model PFL-800

Personal Computer Interface
Model PCI-1800

STAR Cryoelectronics

25-A Bisbee Court
Santa Fe, NM 87508
U. S. A.

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Revision Record

Date	Revision	Description
October 3, 2001		Initial Draft
December 7, 2001		Second Draft

TECHNICAL SUPPORT

If you have any questions or comments about this product or other products from STAR Cryoelectronics, please contact:

STAR Cryoelectronics

25-A Bisbee Court
Santa Fe, NM 87508
U. S. A.

http://www.starcryo.com/

Technical Support:

Tel.: (505) 424-6454
FAX: (505) 424-8225
Email: info@starcryo.com

WARRANTY

STAR Cryoelectronics Limited Warranty

STAR Cryoelectronics warrants this product for a period of twelve (12) months from date of original shipment to the customer. Any part found to be defective in material or workmanship during the warranty period will be repaired or replaced without charge to the owner. Prior to returning the instrument for repair, authorization must be obtained from STAR Cryoelectronics or an authorized STAR Cryoelectronics service agent. All repairs will be warranted for only the remaining portion of the original warranty, plus the time between receipt of the instrument at STAR Cryoelectronics and its return to the owner.

This warranty is limited to STAR Cryoelectronics products that are purchased directly from STAR Cryoelectronics, its OEM suppliers, or its authorized sales representatives. It does not apply to damage caused by accident, misuse, fire, flood or acts of God, or from failure to properly install, operate, or maintain the product in accordance with the printed instructions provided.

This warranty is in lieu of any other warranties, expressed or implied, including merchantability or fitness for purpose, which are expressly excluded. The owner agrees that STAR Cryoelectronics' liability with respect to this product shall be as set forth in this warranty, and incidental or consequential damages are expressly excluded.

SAFETY PRECAUTIONS

Do remove product covers or panels except for modifications as specified in this manual.

Do not operate without all covers and panels in place.

Do not attempt to repair, adjust, or modify the instrument, except for modifications as specified in this manual. This could cause nullification of any warranty. For service, return the instrument to STAR Cryoelectronics or any authorized representative.

DO NOT OPERATE THIS INSTRUMENT IN A VOLATILE ENVIRONMENT, SUCH AS IN THE PRESENCE OF ANY FLAMMABLE GASES OR FUMES.

1 MODEL PFL-800 PROGRAMMABLE FEEDBACK LOOP

The Model PFL-800 Programmable Feedback Loop (PFL) may be used to control up to eight independent dc SQUID channels. The PFL is designed using three 12-bit octal digital-to-analog converters (DACs), which provide independent, high-resolution bias current, modulation and dc flux offset for up to eight dc SQUIDs. Four feedback ranges are supported, ±1, ±10, ±100 and ±1000 Φ_0 full scale for dc SQUIDs with nominally 10 $\mu A/\Phi_0$ feedback coupling. Fast resets within a few microseconds may be executed manually by injecting a TTL signal into a remote reset port, or the PFL may be configured to automatically reset any channel whose output signal approaches full scale. The three drive signals and feedback range for each SQUID may be remotely configured via software.

A digital interface based on a programmable gate array is included in the PFL. The digital interface is designed using STAR Cryoelectronics' Serial Control Code (SCC) architecture. A transmitter for the SCC is located in a separate personal computer interface (PCI) Model PCI-1800, which also provides DC power to operate the PFL. Communication with the PCI is accomplished using either a parallel port or standard RS-232C port on an IBM-compatible personal computer. The 32-bit SCC includes a 5-bit address enabling multiple PFLs (up to 28 PFLs corresponding to 224 SQUID channels) to be addressed independently. The analog output signals of all eight SQUIDs are available at a 25-pin D-connector on the rear panel of the PCI-1800 for digitization using an external data acquisition (DAQ) system.

1.1 Preamplifier and Transformer Coupling

The first stage of the PFL preamplifier consists of a matching transformer and trans-conductance amplifier circuit based on a low-noise field-effect transistor (FET). The voltage noise referred to the input of the trans-conductance amplifier circuit is about 1 $nV/Hz^{½}$.

The matching transformer may be configured for single- or dual-transformer coupling by installing appropriate jumpers on the PFL printed circuit board. For the single transformer configuration, a transformer with a turns ratio of 25:1 located within the PFL-800 is used, and the voltage leads of the SQUID are ac-coupled to this transformer through a capacitor. In the dual transformer configuration, a "cold" transformer mounted in the sensor package with a turns ratio of 5:1 is used in addition to a 5:1 transformer in the PFL-800. In either configuration, the effective transformer turns ratio is 25, so the voltage noise referred to the input of the matching transformer is better than 40 $pV/Hz^{½}$. For a SQUID with 100 $\mu V/\Phi_0$ transfer function, this corresponds to 0.4 $\mu\Phi_0/Hz^{½}$ flux noise. The PFL-800 is normally factory configured for conventional two-transformer input coupling unless specified otherwise by the customer.

1.2 Multiplier

The preamplifier output feeds one differential input of a multiplier, and a 256 kHz reference square wave signal is applied to the other differential input. The multiplier is configured to accommodate a maximum input signal of ±12.5V.

The multiplier has an intrinsic voltage noise referred to its output of 0.8 μV/Hz^{½} at 1 kHz and 1.2 μV/Hz^{½} at 10 Hz. The multiplier noise contribution at this stage is about 0.05 $\mu\Phi_0$/Hz^{½} at 10 Hz for a SQUID with 100 μV/Φ_0 transfer coefficient and therefore is negligible.

1.3 Integrator

The multiplier output is followed by an integrator circuit. For small signals, the -3dB cut-off frequency $f_{\text{-3dB}}$ is given by the following expression:

$$f_{-3\text{dB}} = \left(\frac{\partial V}{\partial \Phi}\right)_{\text{m}} \cdot \frac{M_m}{2\pi\tau R_{\text{fb}}}$$

where $(\partial V/\partial\Phi)_{\text{m}}$ is the sensor flux-to-voltage transfer function referred to the multiplier output, τ is the integrator time constant, R_{fb} is the feedback resistor selected, and M_m mutual inductance of the modulation coil. The integrator time constant τ is switched along with the feedback resistor R_{fb} in order to maintain constant bandwidth for each of the four PFL sensitivity ranges. The time constants for the HIGH, MEDIUM, LOW and COARSE ranges are 1τ, 10τ, 100τ and 1000τ, respectively, where τ = 5 μs.

In the TUNE mode, the integrator serves as a unity gain inverting amplifier enabling the *V*-Φ characteristic of the SQUID to be observed at the PFL analog output. This mode is used to tune the SQUID to locate the optimal working point.

1.4 Reset

Shunting the integrator capacitance resets the feedback loop. This action is initiated remotely via the SQUID Control Module software, or a TTL signal may be injected into the external reset port on the rear panel of the PC Interface. Briefly, when the external TTL reset signal goes "HI," the feedback loop is opened; when the TTL signal goes "LO," the loop is closed. The minimum time required to execute software reset via the SQUID Control Module is about 50 μs. If faster reset times are required, the external reset option should be used. Using a TTL signal and the external reset option reset times of less than 5 μs can be achieved.

An optional automatic reset feature is available for the PFGL-800. The optional auto-reset board plugs into a socket on the PFL-800 board and includes separate comparators for each SQUID channel, which automatically resets any of the eight SQUID channels whenever an output signal approaches full scale (±10V). Reset time in this mode does not exceed 1 μs.

1.5 Feedback Circuit

The feedback circuit is designed for dc SQUIDs with a nominal feedback coupling of 10 μA/Φ_0. Four feedback sensitivity ranges are provided via four feedback resistors installed in the PFL-800 according to the following scheme: the feedback resistors for the sensitivity ranges HIGH, MEDIUM, LOW and COARSE are equal to 1 MΩ, 100 kΩ 10 kΩ and 1 kΩ, respectively, corresponding to PFL gains are 10 V/Φ_0, 1 V/Φ_0, 100 mV/Φ_0 and 10 mV/Φ_0, and full-scale ranges of ±1, ±10, ±100 and ±1000 Φ_0. The

exact values are sensor-specific and must be determined or calibrated by the user. The feedback sensitivity range may be selected remotely via the SQUID Control Module.

Table 1-1 Feedback resistors, feedback loop gain, and full scale ranges for the four feedback sensitivity ranges.

Range	HIGH	MEDIUM	LOW	COARSE
Rfb	1 MΩ	100 kΩ	10 kΩ	1kΩ
Gain	10 V/Φ_0	1 V/Φ_0	100 mV/Φ_0	10 mV/Φ_0
Full Scale	±1 Φ_0	±10 Φ_0	±100 Φ_0	±1000 Φ_0

The three highest sensitivity ranges are designed using high-stability 25 ppm/°C resistors in order to minimize the SQUID feedback circuit thermal drift. The COARSE sensitivity range uses standard 100 ppm/°C resistors.

The feedback current is supplied differentially to the sensor. The feedback circuit noise contribution to the SQUID feedback coil depends on the sensitivity range and is less than: 60 pA/Hz^{½}, 6 pA/Hz^{½}, 0.6 pA/Hz^{½} and 0.06 pA/Hz^{½} at 1Hz for the COARSE, LOW, MEDIUM and HIGH ranges respectively. Thus, even for operation using the LOW range, which corresponds to 100 mV/Φ_0 sensitivity, the total noise contribution from the feedback circuit will not exceed 0.6 μΦ_0/Hz^{½} for a SQUID with 10 μA/Φ_0 feedback coupling and therefore is negligible.

The sixth position of a six-pole DIP switch inside the PFL-800 configures the phase (0° or 180°) of the modulation reference signal for all eight channels. This switch is used to reverse the phase of the modulation reference signal, which inverts the lock point on the SQUID V-Φ characteristic for flux locked-loop operation. As the optimal lock point may vary from SQUID to SQUID, the noise performance and tune parameters should be checked for each switch position in order to determine the best setting. The bottom cover of the PFL-800 must be removed to access this switch.

1.6 Bias, Modulation and DC Flux Offset Drivers

The differential bias, modulation and dc flux offset signals are derived from three 12-bit digital-to-analog converters (DAC) controlled by a field programmable gate array (FPGA). All signal levels are set remotely via the SQUID Control Module. Owing to the high resolution of the DAC used, all signal ranges have ample headroom so that a wide range of SQUID parameters can be accommodated.

For all drivers, the DAC is used as a digitally controlled voltage divider with a resolution determined by the 12-bit digital code stored in the internal DAC register. The current noise injected by the Modulation, dc Flux Offset and Current Bias circuits into the SQUID modulation coil and the SQUID bias input is < 7 pA/Hz^{½} at 1Hz, which results in an additional SQUID output noise of around 0.8 μΦ_0/Hz^{½} at 1Hz for a SQUID with 100μV/Φ_0 transfer coefficient and therefore is negligible for typical dc SQUID sensors.

1.6.1 Bias Current Driver

The maximum dc bias current is 164 μA, which may be set with the resolution of ±40 nA. The PFL-800 does not support an ac bias mode.

1.6.2 Modulation Driver

The modulation frequency is 256 kHz. The maximum modulation signal is 200 μA_{pp}, which may be set with the resolution of 50 nA_{pp}. The high-frequency, low-noise amplifiers used in the modulation circuit provide close to true square-wave shape of the output modulation pulses, resulting in very small phase shifts between the input and reference signals at the multiplier and therefore increased signal-to-noise ratio of the amplifier. This design eliminates the need for a phase shift compensation circuit for each channel.

1.6.3 DC Flux Offset Driver

The differential current drive used for the dc flux offset allows improved ground noise suppression. This is critical for tightly coupled SQUIDs. The offset range is 164 μA, corresponding to 16.4 Φ_0 for dc SQUIDs with 10 $\mu A/\Phi_0$ feedback coupling.

1.7 External Signal Input

The external signal input allows the user to inject an external signal into the SQUID feedback coil. For example, a test waveform may be injected to tune the SQUID with the PFL set in the TUNE mode, or the external signal input may be used in conjunction with electronic noise suppression techniques such as the formation of electronic gradiometers.

The external signal is coupled differentially to the SQUID feedback coil through four pairs of matched resistors, 1 kΩ, 10 kΩ, 100 kΩ and 1 MΩ, in order to accommodate four different input sensitivity ranges of 1000 $\mu A/V_{in}$, 100 $\mu A/V_{in}$, 10 $\mu A/V_{in}$ and 1 $\mu A/V_{in}$, respectively. The input sensitivity range is selected remotely via the SQUID Control Module.

1.8 Buffered Analog Output

The analog PFL-800 output is a true differential output. It is buffered using two low-noise, low-drift operational amplifiers, capable of driving a large capacitive load, with an output signal range of ±11 V.

1.9 Heater

The heater circuit consists of a 100 mA current generator for each channel, which provides a constant 100 mA current for heater resistors up to 100 Ω. When the heater is enabled via the SCC interface, the heater LED on the PFL is activated and a 100 mA current is applied to the heater resistor in the SQUID sensor package. Only one heater may be activated at a time. The duration of the heater current is limited to 1/2 second, unless the heater is reactivated via the SCC interface. This feature is a safety precaution, which eliminates the potential for damage to the sensor in case of a computer malfunction. When the heater is disabled, the heater LED is de-activated and the disabled heater output is grounded. This eliminates the RF noise contribution from the heater wires into the SQUID feedback coil.

1.10 PFL Hardware Address and Digital Interface

The 5-bit hardware address of each PFL is configured by manually setting a 6-pole DIP switch inside the PFL to the binary representation of the address. The sixth pole is used to reverse the phase of the modulation reference signal, which inverts the lock point on the SQUID V-Φ characteristic for flux locked-loop operation (see Sec. 1.5). Valid PFL addresses are in the range 0 – 8, corresponding to SQUID Channels 1 - 223. The bottom cover of the PFL-800 must be removed to access the switch to change the address. ***NOTE: The switch positions labeled "ON" on the DIP switch represent binary 0, NOT binary 1!*** The position labeled "1" represents the least significant bit (decimal 1), the position labeled "2" represents the second least significant bit (decimal 2), and so on. Thus, for example, the PFL-800 for SQUID Channels 1 – 8 should be configured with address 0 (the first five poles set to the ON (binary 0) position), the PFL-800 for SQUID Channels 9 – 16 should be configured with address 1 (the first pole OFF (binary 1) and all others set to ON (binary 0)), etc.

The SCC receiver circuitry inside the PFL-800 is implemented using a field programmable gate array (FPGA). Other ICs are used for work with mixed analog and digital signals that cannot be implemented with the FPGA.

1.11 LED Indicators

There are three LEDs on the PFL-800 front panel: DATA, FAULT, HEATER. The red FAULT LED will blink once at power up, while the green DATA LED lights when a command is sent to a given PFL-800, thereby confirming that proper communication is established. In the event there is a problem with code transmission, the red FAULT LED will turn on. The yellow HEATER LED turns on whenever the heater for one of the SQUID channels is activated.

1.12 PFL-800 Connector Pinouts

1.12.1 SENSOR

The following table specifies the pin assignments at the 68-pin SCSI connector for sensor inputs. Refer to the key below for the abbreviations used in the table.

Pin	Function	Pin	Function	Key	
1	V1H	35	V1L	V*n*H	Voltage, Ch. *n*, High
2	M1H	36	M1L	V*n*L	Voltage, Ch. *n*, Low
3	B1H	37	B1L	M*n*H	Modulation, Ch. *n*, High
4	V2H	38	V2L	M*n*L	Modulation, Ch. *n*, Low
5	M2H	39	M2L	B*n*H	Bias, Ch. *n*, High
6	B2H	40	B2L	B*n*L	Bias, Ch. *n*, Low
7	V3H	41	V3L	Htr*n*H	Heater, Ch. *n*, High
8	M3H	42	M3L	Htr*n*L	Heater, Ch. *n*, Low
9	B3H	43	B3L		
10	V4H	44	V4L		
11	M4H	45	M4L		
12	B4H	46	B4L		
13	V5H	47	V5L		
14	M5H	48	M5L		
15	B5H	49	B5L		
16	V6H	50	V6L		
17	M6H	51	M6L		
18	B6H	52	B6L		
19	V7H	53	V7L		
20	M7H	54	M7L		
21	B7H	55	B7L		
22	V8H	56	V8L		
23	M8H	57	M8L		
24	B8H	58	B8L		
25	GND	59	GND		
26	GND	60	GND		
27	Htr1H	61	Htr1L		
28	Htr2H	62	Htr2L		
29	Htr3H	63	Htr3L		
30	Htr4H	64	Htr4L		
31	Htr5H	65	Htr5L		
32	Htr6H	66	Htr6L		
33	Htr7H	67	Htr7L		
34	Htr8H	68	Htr8L		

1.12.2 PCI

The following table specifies the pin assignments at the 68-pin SCSI connector interface to the PCI-1800. Refer to the key below for the abbreviations used in the table.

Pin	Function	Pin	Function
1	+12 VDC	35	+12 VDC
2	+12 VDC	36	+12 VDC
3	-12 VDC	37	-12 VDC
4	-12 VDC	38	-12 VDC
5	Analog Ground	39	Analog Ground
6	Analog Ground	40	Analog Ground
7	Analog Ground	41	VCC
8	VCC	42	VCC Sense
9	XRST8H	43	XRST8L
10	XRST7H	44	XRST7L
11	XRST6H	45	XRST6L
12	XRST5H	46	XRST5L
13	XRST4H	47	XRST4L
14	XRST3H	48	XRST3L
15	XRST2H	49	XRST2L
16	XRST1H	50	XRST1L
17	SCCL	51	SCCH
18	CLKINL	52	CLKINH
19	OUT8H	53	OUT8L
20	TEST8H	54	TEST8L
21	OUT7H	55	OUT7L
22	TEST7H	56	TEST7L
23	OUT6H	57	OUT6L
24	TEST6H	58	TEST6L
25	OUT5H	59	OUT5L
26	TEST5H	60	TEST5L
27	OUT4H	61	OUT4L
28	TEST4H	62	TEST4L
29	OUT3H	63	OUT3L
30	TEST3H	64	TEST3L
31	OUT2H	65	OUT2L
32	TEST2H	66	TEST2L
33	OUT1H	67	OUT1L
34	TEST1H	68	TEST1L

Key	
XRST*n*H	Ext. Reset, Ch. *n*, High
XRST*n*L	Ext. Reset, Ch. *n*, Low
SCCH	Serial Control Code, High
SCCL	Serial Control Code, Low
CLKINH	Clock In, High
CLKINL	Clock In, Low
OUT*n*H	Output, Ch. *n*, High
OUT*n*L	Output, Ch. *n*, Low
TEST*n*H	Test Sig. Input, Ch. *n*, High
TEST*n*L	Test Sig. Input, Ch. *n*, Low

1.13 PFL-800 Specifications (Preliminary)

No. of Channels	Eight independent SQUID channels, remotely controllable.
Remote Control	PC-based, proprietary Serial Control Code (SCC) interface
	5-bit internally configurable hardware address
	Up to 28 eight-channel PFLs (224 SQUID channels) may be controlled independently
Sensor Types	LTS
SQUID Inputs	Via 68-pin SCSI connector
Input Coupling	Single (warm) or Dual (warm plus cooled) input transformer options, configurable via internal solder jumpers
Bias	0 - 160 µA DC, 1 part in 4096 resolution
Modulation	0 - 200 μA_{p-p}, 1 part in 4096 resolution, provided by internal 256 kHz generator referenced to external clock signal from PC Interface
Feedback	Internal or External
Ranges	Four feedback ranges, remotely configurable
	±10 µA, HIGH Sensitivity Mode, max. 0.5 nA/°C drift
	±100 µA, MEDIUM Sensitivity Mode, max. 5 nA/°C drift
	±1 mA, LOW Sensitivity Mode, max. 50 nA/°C drift
	±10 mA, COARSE Sensitivity Mode, max. 2 µA/°C drift
Integrator	5 µs, 50 µs, 500 µs, 5 ms time constants, remotely configurable
Reset	Via software or external TTL signal
	External reset time <5µsec
	Optional auto-reset function
DC Offset	160 µA, 1 part in 8192 resolution, max. 2.5 nA/°C drift
	1 nA_{p-p} drift over 24 hours typical.
Bandwidth	Up to 100 kHz depending on SQUID transfer coefficient $\partial V/\partial \Phi$
SQUID Outputs	±10 V differential analog outputs for each channel
Test Signal Inputs	Differential; 1 mV/µA, 10 mV/µA, 100 mV/µA, 1V/µA,
	remotely configurable for each channel,
	10 mA maximum current, 10 kΩ input impedance
Remote Interface I/O	Via 68-pin SCSI connector; includes all SQUID outputs, test signal inputs, SCC data, power, and grounds
Indicators	SCC DATA OK/Fault Status LEDs, Heater LED
Sensor Heater Supply	100 mA current source for heater resistances up to 75 Ω
Power Requirements	+12 VDC, 436 mA (+100 mA per activated heater), -12 VDC, 376 mA, +5 VDC, 45 mA (+11 mA per activated heater)
Size (W×H×D)	$9.88 \times 7 \times 0.94$ (inch) ($251 \times 178 \times 24$ (mm))
Weight	2.8 lb (1270 g)

2 MODEL PCI-1800 MULTICHANNEL PC INTERFACE

The Personal Computer Interface Model PCI-1800 serves as computer interface for communications from an IBM-compatible PC to the Model PFL-800 Programmable Feedback Loop. The following are standard features of the PCI-1800:

- Front panel status indicator LEDs.
- Integral ±12 VDC power supply or optional battery power input.
- Integral STAR Cryoelectronics Serial Control Code (SCC) transmitter for uni-directional communications with PFL-800.
- Internal test signal generator with adjustable amplitude and frequency.
- Internal clock generator for PFL-800.
- Optoisolated synchronization output for test signal to simplify triggering when an external oscilloscope is used.
- Remotely controlled multiplexer to enable internal or external test signal coupling to each SQUID channel for tuning.
- Optional remotely configurable 4-pole low-pass Butterworth filters for all eight analog output signals.
- Remotely selectable reference voltage or ground for each channel for data acquisition calibration.
- Optoisolated, fast external TTL reset port for each SQUID channel.
- Optoisolated SCC Input and SCC Output to enable any PCI-1800 to drive any number of PCI-1800 slaves in a daisy-chain configuration.

2.1 PCI-1800 Front Panel Description

Located on the front panel of the PCI-1800 are the main power switch with embedded indicator, a TEST INPUT BNC, WIDEBAND and FILTERED output BNCs, and three status indicator LEDs.

The user may remotely select which analog output is available at the front panel of the PCI-1800. For the FILTERED output, the user may remotely select one of four optional 4-pole Butterworth filters with cutoff frequencies of 3, 6, 15 or 30 MHz (Frequency Devices Model D74L4B 16-pin DIP anti-alias filter), or unfiltered for wideband. The unfiltered, wideband analog output of the selected PFL is always available at the WIDEBAND BNC.

The user may inject a test signal from an external source to any remotely selected channel via the TEST INPUT BNC. The external signal may be enabled or disabled remotely.

Three LED indicators on the front panel of the PCI-1800 provide interface status information for the user. The READY indicator is activated when the proper interface with the host PC is established and power to the PCI-1800 is switched on. If no signal is present at the SCC INPUT on the rear panel, the PCI-1800 auto-recognizes it is the

master interface and the MASTER indicator LED is activated. The DATA indicator flashes whenever SCC data is sent to any PFL.

2.2 PCI-1800 Rear Panel Description

A 68-pin SCSI connector on the rear panel of the PCI-1800 is used to interface to the PFL-800. The connector pinout is given in Section 2.4.1.

Two DB-25 connectors are located in the middle of the rear panel. The DB-25 male INPUT connector may be used to connect an external test or feedback signal to any of the eight PFL channels. Such signals may be used, for example, to tune a selected SQUID, to form electronic gradiometer configurations, or for filtering. All inputs are differential. The input resistance is 5 kΩ, and the linear range of the input voltage is ±10 V. The maximum allowable input voltage is ±12 V. The pinout of the 25-pin INPUT connector is given in Section 2.4.2.

The analog outputs of all eight channels are available at the DB-25 female OUTPUT connector. This port is used to interface with the optional Data Acquisition system (DAQ). The linear range of the output signals is ±10 V, but the amplitudes of the output signals can reach ±12 V. The output resistance is 620 Ohm, and the maximum load capacitance is 10 nF. The pinout of the 25-pin OUTPUT connector is given in Section 2.4.3.

The shells of the INPUT and OUTPUT connectors as well as the 68-pin PFL connector are connected to the analog signal ground of the PCI-1800, which is isolated from the chassis.

A fast external reset of any channel may be executed by injecting a TTL signal into the appropriate pin on the DB-9 male EXT RESET connector where it is passed directly to the corresponding SQUID channel in the PFL-800. Since the reset function is implemented in hardware, fast reset times of <5 µs are possible. A TTL “HI” signal discharges the integrator and opens the feedback loop, and a TTL “LO” signal restores normal feedback operation. The voltages of the TTL signal must be in the range -0.5 V min. to +5.5 V max. to avoid damage to the external reset circuit. The pinout of the 9-pin EXT RESET connector is given in Section 2.4.4.

The SCC IN and SCC OUT 1-pin LEMO connectors are used to connect any number of slave interfaces to a master PCI-1800. Each interface auto-recognizes whether it is a master or slave. For the master interface, the MASTER indicator LED on the front panel is activated.

The CLOCK IN and CLOCK OUT 1-pin LEMO connectors are used to synchronize the clock signals of multiple PCI-1800 units operated in master/slave mode.

A synchronization signal derived from the PCI-1800 internal signal generator is available at the SYNC OUT BNC. This synchronization signal may be used to simplify triggering when using an oscilloscope or the optional Data Acquisition system to monitor the PFL analog outputs.

The EXT RESET, SCC IN, SCC OUT and SYNC OUT connectors are all grounded to the PCI-1800 chassis. Each is optoisolated from the PCI-1800 analog signal ground.

An IBM-compatible PC is used for uni-directional communications with the PCI-1800. The DB-25 male PARALLEL PORT connector may be used to interface to a standard parallel port on the PC, or the DB-25 female RS-232 connector may be used with a standard RS-232C interface. The PARALLEL PORT and RS-232 interface may not be used simultaneously. For multi-unit operation, only the master unit should be connected to the PC communication port.

The ac power entry module allows the user to select the proper operating voltage depending on the available mains voltage. Included in the module are rf filters and a fuse.

The optional BATTERY port is used to power the PCI-1800 and PFL-800 using an external power source. The required chassis-mount connector assembly and installation instructions are available from STAR Cryoelectronics.

To change the fuse in the PCI-1800, remove the power cord from the unit. The plastic part with the fuse icon is the fuse holder, which should be pulled outward away from the unit to remove. You may find it necessary to use a screwdriver to pry the fuse holder loose.

2.3 Changing the Address and Filters in the PCI-1800

The address of the PCI-1800 is set using an 8-pole DIP switch inside the unit. To change the address, make sure the power cord is disconnected from the PCI-1800 and remove the top cover. Locate the address switch on the main printed circuit board, as shown in Figure 2-1. Set the switch to the binary representation of the address, noting that the position marked as ON corresponds to a binary “0”. The pole marked “1” is the least significant bit, and the pole marked “7” is the most significant bit (128 decimal). Valid PCI-1800 addresses range from 224 to 252. Thus, the first PCI-1800 unit (SQUID channels 1 to 8) should be set with the first five switches in the OFF position and the last three switches in the ON position (00000111 binary), while the second PCI-1800 unit (SQUID channels 9 to 16) should be set with the first and last three switches in the ON position and the second through fifth switches in the OFF position (binary 1000011), etc..

The PCI-1800 may be configured with up to four optional 4-pole Butterworth low-pass filters (Frequency Devices D74L4B-series) per channel. If ordered at time of purchase, the filters are installed at the factory. If purchased at a later time, or if your application requires different filter characteristics, the filters may easily be installed or replaced by the user. Contact STAR Cryoelectronics or Frequency Devices about obtaining replacement or substitute filters.

To replace or install a filter, make sure the power cord is disconnected from the PCI-1800 and remove the top cover. The filters are located on the printed circuit board as shown in Figure 2-1. Locate the position of the filter you wish to install or replace. To remove a filter, pull the filter straight up out of its mounting socket, directly away from the circuit board so as not to bend the pins on the filter. Installation of a filter is the reverse of its removal, taking care to orient the filter properly as shown at the bottom of Figure 2-1.

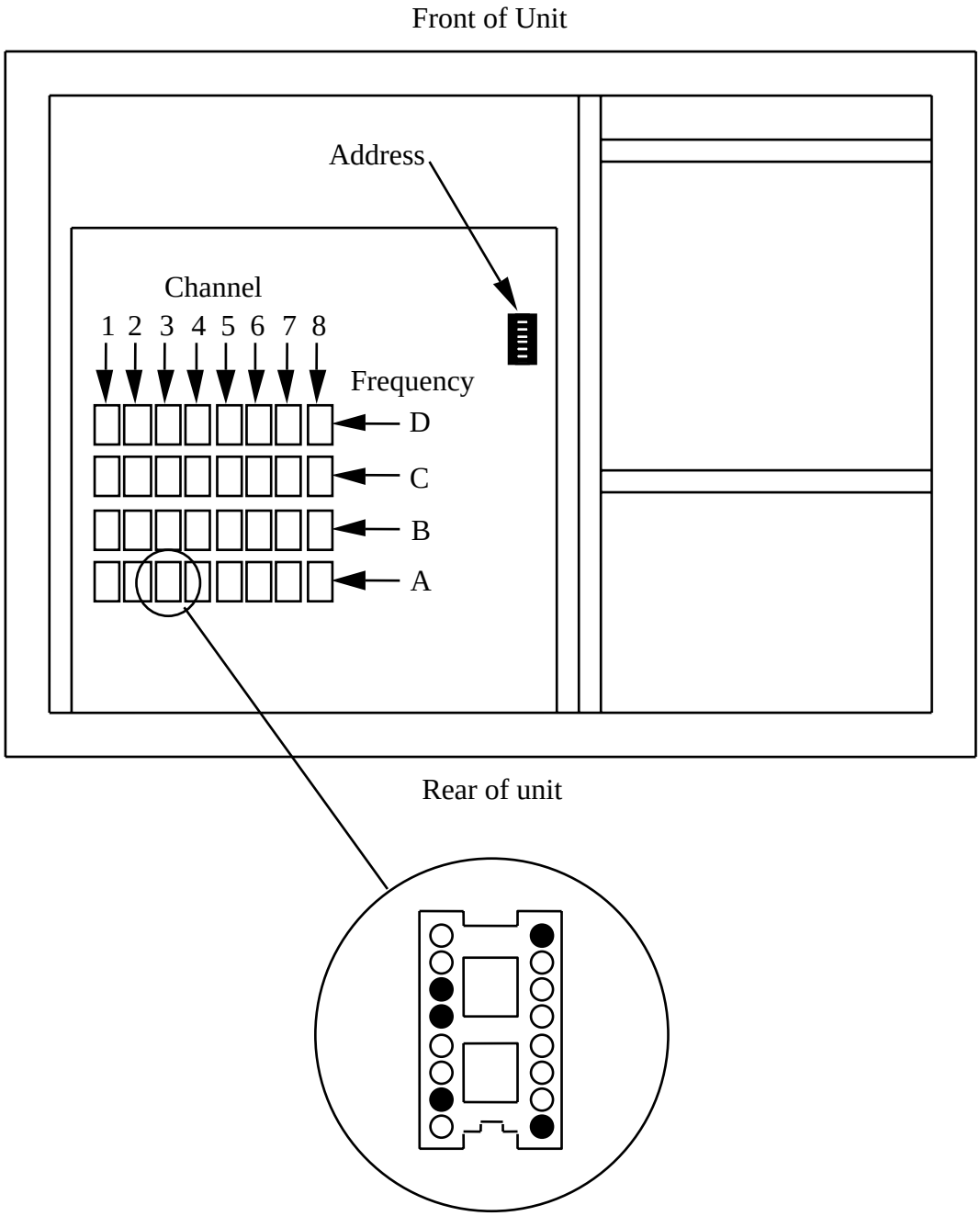

Figure 2-1 Schematic drawing of the inside of PCI-1800 viewed from above showing the locations of the signal filters and address switch. Note that the polarity of the address switch is reversed such that ON represents a binary “0” (see text). Four filters (A, B, C, D) may be installed for each channel. The proper insertion orientation for the filters is indicated at the bottom of the Figure. The sockets drawn as filled circles in the Figure indicate where filter package pins plug in (see text).

2.4 PCI-1800 Rear Panel Connector Pinouts

2.4.1 PFL

The following table specifies the pin assignments at the 68-pin SCSI connector interface to the PFL-800. Refer to the key below for the abbreviations used in the table.

Pin	Function	Pin	Function	Key	
1	+12 VDC	35	+12 VDC	XRST*n*H	Ext. Reset, Ch. *n*, Hi
2	+12 VDC	36	+12 VDC	XRST*n*L	Ext. Reset, Ch. *n*, Low
3	-12 VDC	37	-12 VDC	SCCL	Serial Control Code, Low
4	-12 VDC	38	-12 VDC	SCCH	Serial Control Code, Hi
5	Analog Ground	39	Analog Ground	CLKOUTL	Clock Out, Low
6	Analog Ground	40	Analog Ground	CLKOUTH	Clock Out, Hi
7	Analog Ground	41	VCC	OUT*n*H	Output, Ch. *n*, Hi
8	VCC	42	VCC Sense	OUT*n*H	Output, Ch. *n*, Low
9	XRST8H	43	XRST8L	TEST*n*H	Test Sig. Output, Ch. *n*, Hi
10	XRST7H	44	XRST7L	TEST*n*H	Test Sig. Output, Ch. *n*, Low
11	XRST6H	45	XRST6L		
12	XRST5H	46	XRST5L		
13	XRST4H	47	XRST4L		
14	XRST3H	48	XRST3L		
15	XRST2H	49	XRST2L		
16	XRST1H	50	XRST1L		
17	SCCL	51	SCCH		
18	CLKOUTL	52	CLKOUTH		
19	OUT8H	53	OUT8L		
20	TEST8H	54	TEST8L		
21	OUT7H	55	OUT7L		
22	TEST7H	56	TEST7L		
23	OUT6H	57	OUT6L		
24	TEST6H	58	TEST6L		
25	OUT5H	59	OUT5L		
26	TEST5H	60	TEST5L		
27	OUT4H	61	OUT4L		
28	TEST4H	62	TEST4L		
29	OUT3H	63	OUT3L		
30	TEST3H	64	TEST3L		
31	OUT2H	65	OUT2L		
32	TEST2H	66	TEST2L		
33	OUT1H	67	OUT1L		
34	TEST1H	68	TEST1L		

2.4.2 INPUT

INPUT	DB-25 Connector for PFL input signals
	Pin 1: CH1 External Signal Differential Input (+)
	Pin 2: CH1 External Signal Differential Input (-)
	Pin 3: PCI-1800 Signal Ground
	Pin 4: CH3 External Signal Differential Input (+)
	Pin 5: CH3 External Signal Differential Input (-)
	Pin 6: PCI-1800 Signal Ground
	Pin 7: CH5 External Signal Differential Input (+)
	Pin 8: CH5 External Signal Differential Input (-)
	Pin 9: PCI-1800 Signal Ground
	Pin 10: CH7 External Signal Differential Input (+)
	Pin 11: CH7 External Signal Differential Input (-)
	Pin 12: PCI-1800 Signal Ground
	Pin 13: PCI-1800 Signal Ground
	Pin 14: PCI-1800 Signal Ground
	Pin 15: CH2 External Signal Differential Input (+)
	Pin 16: CH2 External Signal Differential Input (-)
	Pin 17: PCI-1800 Signal Ground
	Pin 18: CH4 External Signal Differential Input (+)
	Pin 19: CH4 External Signal Differential Input (-)
	Pin 20: PCI-1800 Signal Ground
	Pin 21: CH6 External Signal Differential Input (+)
	Pin 22: CH6 External Signal Differential Input (-)
	Pin 23: PCI-1800 Signal Ground
	Pin 24: CH8 External Signal Differential Input (+)
	Pin 25: CH8 External Signal Differential Input (-)

2.4.3 OUTPUT

OUTPUT — DB-25 Connector for PFL output signals

Pin 1: CH1 Single-ended Output
Pin 2: PCI-1800 Signal Ground
Pin 3: PCI-1800 Signal Ground
Pin 4: CH3 Single-ended Output
Pin 5: PCI-1800 Signal Ground
Pin 6: PCI-1800 Signal Ground
Pin 7: CH5 Single-ended Output
Pin 8: PCI-1800 Signal Ground
Pin 9: PCI-1800 Signal Ground
Pin 10: CH7 Single-ended Output
Pin 11: PCI-1800 Signal Ground
Pin 12: PCI-1800 Signal Ground
Pin 13: PCI-1800 Signal Ground
Pin 14: PCI-1800 Signal Ground
Pin 15: CH2 Single-ended Output
Pin 16: PCI-1800 Signal Ground
Pin 17: PCI-1800 Signal Ground
Pin 18: CH4 Single-ended Output
Pin 19: PCI-1800 Signal Ground
Pin 20: PCI-1800 Signal Ground
Pin 21: CH6 Single-ended Output
Pin 22: PCI-1800 Signal Ground
Pin 23: PCI-1800 Signal Ground
Pin 24: CH8 Single-ended Output
Pin 25: PCI-1800 Signal Ground

2.4.4 EXT RESET

EXT RESET	DB-9 Connector for external reset; TTL-compatible input (-0.5 V min. to +5.5 V max.)
	Pin 1: CH 1 External Reset Input (TTL)
	Pin 2: CH 2 External Reset Input (TTL)
	Pin 3: CH 3 External Reset Input (TTL)
	Pin 4: CH 4 External Reset Input (TTL)
	Pin 5: CH 5 External Reset Input (TTL)
	Pin 6: CH 6 External Reset Input (TTL)
	Pin 7: CH 7 External Reset Input (TTL)
	Pin 8: CH 8 External Reset Input (TTL)
	Pin 9: PCI-1800 Chassis Ground

2.4.5 SCC, CLOCK, SYNC, POWER and Communications Ports

SCC IN	1-pin LEMO Coaxial for Serial Control Code input
SCC OUT	1-pin LEMO Coaxial for Serial Control Code output
CLOCK IN	1-pin LEMO Coaxial for clock signal input
CLOCK OUT	1-pin LEMO Coaxial for clock signal output
SYNC OUT	BNC
POWER	IEC 320 Power Entry Module
	Selectable for 110/220 VAC operation
PARALLEL PORT	DB-25 Male connector
RS-232	DB-25 Female connector

2.5 PCI-1800 Front Panel

TEST INPUT	BNC
OUTPUT, WIDEBAND	BNC
OUTPUT, FILTERED	BNC
READY	LED indicator
MASTER	LED indicator
DATA	LED indicator
POWER	Rocker on/off switch with embedded LED indicator

2.6 PCI-1800 Specifications (Preliminary)

No. of Channels	Supports one 8-Channel Model PFL-800 Programmable Feedback Loop
Clock	Internal generator provides clock signal for PFL Master/Slave mode supported to synchronize clock signal for multiple PFLs Slave PCI-1800 auto-recognizes slave mode
Communications	From PC: RS-232 or Parallel Port To PFL: STAR Cryoelectronics Serial Control Code
Analog Outputs	±10 V buffered PFL output Front panel BNC: Wideband or Filtered, remotely configurable for each channel Rear panel DB-25: Eight differential analog outputs for each SQUID channel
Test Signal Input	Front panel BNC: Differential, remotely configurable for each channel, ±10 V max., 50 Ω Rear panel DB-25: Eight differential inputs for each SQUID channel, ±10 V max., 10 kΩ
Test Signal Generator	0 – 2 $V_{p\text{-}p}$, 50 – 5,000 Hz, remotely controllable
External Reset Inputs	TTL (HI resets feedback loop), via rear-panel DB-9 connector
Filters	30, 15, 6, 3 kHz plug-in 4-pole Butterworth (optional)
Power Requirement	120 or 240 VAC (selectable), 50/60 Hz, TBD W, or external battery
Cable Length	Up to TBD m to Programmable Feedback Loop
Size (W×H×D)	16.7 × 1.69 × 12.7 (in) (424 × 44 × 323 (mm))
Weight	7.8 lb (3545 g)

3 PCS800 CONTROL SOFTWARE

The PCS800 Control Software is a 32-bit application that may be used to control up to 28 PFL-800/PCI-1800 units (228 channels) configured in a master/slave mode. Communication to all PFLs is handled by the master PCI-1800, which is interfaced to the PC via the serial or parallel port. The slave PCI-1800 units must be connected in a daisy-chain fashion using the 1-pin LEMO cables provided with the system. To interface the first slave PCI, connect the SCC output on the master PCI to the SCC input on the slave PCI. Similarly, to connect the second slave PCI, connect the SCC output on the first slave PCI to the SCC input on the second slave PCI.

NOTE: The hardware addresses of each PCI and PFL pair must be properly configured. Valid PFL-800 hardware addresses range from 0-27 (corresponding to SQUID channels 1 – 224 (actually 0 – 223, but the software maps the physical SQUID addresses to the range 1 – 224 to simplify channel counting), while valid PCI-1800 hardware addresses range from 224 to 252.